REMARKS

The final Office Action dated March 2, 2004, was carefully reviewed. The Examiner maintained the rejection 9 of claims 1-9 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,138,185 to Nelson et al., hereinafter Nelson. The Examiner also maintained the rejection of claims 10-13 under 35 U.S.C. § 103 as being unpatentable over Nelson in view of Obata.

In the prior response dated January 13, 2004, the present invention was distinguished from Nelson in that Nelson does not disclose using a clock signal to synchronize the operation of the serial I/O shifter as claimed in the present invention. The Examiner indicated that Nelson, at column 4, lines 3-67, teaches serial requests and serial responses can be processed concurrently. In other words, these requests can be processed during a single clock cycle. Thus, the Nelson reference teaches parallel processing so as not to consume connection bus bandwidth. However, it is respectfully asserted that the feature of concurrent processing of requests does not mean that Nelson inherently teaches synchronizing the serial I/O shifter using the clock signal as claimed by the applicants of the present invention. These remarks are presented to further clarify the differences between Nelson and the present invention.

To support the statement that Nelson does not teach synchronizing the operation of the serial I/O shifter using the clock signal, reference is made to Figure 4 of Nelson. Figure 4 shows two concurrent request messages together with a concurrent response message, but these messages are in operation asynchronous with respect to each other and may or may not occur concurrently. Nelson teaches

that no mandatory timing relationship is implied between the connection and response busses. (See column 5, lines 30-40).

Applicants' independent claim 1 requires synchronizing the operation of the I/O shifter using the clock signal and the latch signal. Similarly, independent claim 5 serializes parallel data and requires serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal. It is respectfully asserted that these features are not disclosed in Nelson.

According to the present invention, the software is responsible for the control of each serial I/O shifter and each I/O shifter can be enabled or disabled any time through software commands. The operation of all the serial I/O shifters is synchronized to their respective clock and latch signals. The operation of the serial I/O shifters becomes transparent to the software, and once the shifters are enabled, their operation is autonomous.

Nelson discloses a clock signal coupled to each PRC and each port. However, the clock signal in Nelson does not synchronize I/O shifters as taught by the present invention. And further, Nelson teaches no mandatory timing relationship between the connection and response busses. The serial request and response busses in Nelson operate independently in a non-blocking fashion to process connection and clear requests in parallel. Nelson teaches asynchronous operation. This is significantly different from the present invention.

The present invention provides a user with the capability to serially transfer selected I/O signals with other system devices while using one of several different serial timing protocols, which were designed to accommodate a variety of serial device interfaces. The present invention synchronously transfers serial data and reconstructs parallel I/O signals from an incoming serial data stream.

According to the present invention, the operation of all of the serial I/O shifters is synchronized to their respective SCLK and SLATCH signals, as a result, when more than one shifter is associated with a single clock and latch signal, data of all of the serial I/O shifters related to that particular SCLK signal and SLATCH signal are serialized, and de-serialized, in parallel.

It is respectfully asserted that the present invention is not anticipated by the Nelson reference. In light of this further explanation, tt is respectfully requested that the Examiner withdraw the rejection of claims 1-9 under 35 U.S.C. § 102.

The Examiner also maintained the rejection of claims 10-13 under 35 U.S.C. § 103 as being unpatenable over Nelson in view of U.S. Patent No. 6,301,509 to Obata. The Examiner asserted that Nelson discloses all of the limitations of claim 10 except reconstructing the serial data into parallel I/O signals in a serial I/O shifter. The Examiner asserted that it would have been obvious to combine Nelson with Obata to achieve the present invention. Again, it is respectfully asserted that Nelson does not disclose all of the limitations of the present invention, and therefore, even if combined with Obata, it would not result in the present invention.

The present invention is directed to the problem of design inflexibility for I/O usage. The present invention allows a designer to independently select I/O signals for serial transfer and I/O signals for parallel transfer using several different serial timing protocols. The present invention teaches reconstructing serialized data for communication with a parallel device. Parallel reconstruction begins on the assertion of a latch signal to the external device. Thereafter, serial I/O data from the external device is clocked into the serial I/O shifter. Once all "n" bits of the serial I/O data stream have been clocked into the shifter, the shifter reconstructs the serial data into parallel I/O signals. The parallel I/O signals are then output to the I/O crossover-switching network.

Nelson is directed to the problem of blocked port requests for multi-port connection devices. Nelson proposes a switch that couples a plurality of port request controllers (PRCs) to its own I/O port. A plurality of serial request busses is arranged such that each serial request bus is coupled to each PRC with its associated I/O port. A plurality of serial response busses is coupled such that each serial response bus is coupled to each PRC with its associated port. Nelson teaches processing multiple requests for connection concurrently, or in a parallel fashion, but does not teach serialization of parallel data or reconstruction of serial data into parallel data as taught by the Applicant of the present invention.

The present invention teaches serialization and de-serialization that is synchronized to the clock cycle. For serialization, the signals are sampled on the first edge of the latch signal and transferred at the rate of one bit per clock cycle. For de-serialization, parallel reconstruction begins on the latch signal. Thereafter, serial I/O

data is clocked into the serial I/O shifter from the external device into the serial I/O shifter at the rate of one bit per clock cycle. Nelson specifically discusses the fact that no mandatory timing relationship is implied and that concurrent request messages are in operation asynchronous with respect to each other.

Obata discloses a serial communication circuit that converts parallel signals from the CPU to serial signals that are sent to a control unit. But does not teach synchronization of a plurality of I/O shifters as taught by the present invention, nor does Obata teach synchronized reconstruction of a serial I/O data stream into parallel I/O.

It is respectfully asserted that merely combining Nelson and Obata would not result in the Applicant's invention. Nelson teaches processing connection and clear requests concurrently to avoid blocking signals at busy ports. The clock signal is Nelson is used to encode requests and is not used to synchronize the I/O shifter as claimed in the present invention. Obata discloses a serial communication circuit that converts parallel signals output from the CPU into serial signals. Because Nelson does not teach synchronization of the clock signal and the I/O shifter, the combination of Nelson and Obata would not result in a synchronous transfer of serial data and reconstruction of parallel I/O signals from an incoming serial data stream as taught by the applicant of the present invention.

Should the Examiner have any questions or comments that may place the application in better condition for allowance, he is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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